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Engineering Note

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Project: Central Fiber Tracker
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Subject: Extracting time-of-flight (Z position) from CFT fibers using the AFE I

Introduction

Tracking algorithms within the Central Fiber Tracker suffer from information overload caused by the inherently two-dimensional view of the tracker currently used. Although the discriminator information from the AFE certainly indicates which fibers have been hit, with the exception of the axial Central Preshower fibers there is no direct time-of-flight information available. Analysis of the stereo fibers can yield this information but extracting out valid data from the stereo is a difficult task at best, becoming increasingly more difficult as the luminosity increases.

Although it is the plan and fervent hope that the accelerator will soon move to interactions every 132 nanoseconds, the time afforded by 396 nanosecond operation can be put to good use in the current AFE board to obtain some Z axis information using the current hardware. This document will detail a method by which the current board, with only PLD firmware changes, can be used to extract some Z information from the tracker.

The reader is reminded that the discussion within this document applies to the AFE I, the currently installed boards in the CFT. The current experimental plan is to replace the AFE I by new boards with a different discriminator chip at some point in the future. This is because the discriminator ASIC of the AFE I – the SIFT – is too slow to work at 132 nanosecond interaction rates. The algorithms discussed herein are specific to the SIFT chip and do not apply to any new "AFE 2" board.

Hardware Architecture

A very short review of the hardware in the AFE is useful. Charge entering the board every 396 nanoseconds is integrated by the SIFT chips. The discriminator outputs of the SIFT are sampled by two CPLDs in parallel, the VSVX_MUX and the LVDS_MUX. The VSVX_MUX repacks the discriminator data into byte-wide chunks for later inclusion into the SVX readout that occurs in response to a Level 1 Accept. The LVDS_MUX packs the discriminator data into gigabit links that send the discriminator patterns to the Digital Front End (DFE) boards which do the track recognition used in trigger formation.

Proposed Implementation

The SIFT chip uses a number of clock signals to define the charge integration window. In present usage the beginning of the window is defined by the falling edges of the PRST & DRST clocks, and the end of the window is defined by the rising edge of the S/H clock. S/H is used in two different parts of the SIFT. In the discriminator section, S/H allows the output of the discriminator to be sampled by a small capacitor when high. When S/H goes low, whatever voltage is on the capacitor then drives only a high-impedance buffer such that the output of the SIFT is 'latched'. In the charge transfer section of the SIFT, S/H high causes the output of the preamplifier, as buffered by source followers, to charge a holding capacitor prior to using the READ clock to connect the capacitor to the SVX.

Normally the S/H is a short pulse and the CPLDs sample the output of the discriminator after the pulse, utilizing the SIFT as a latch. If the S/H is held high during most of the integration window, its functionality changes to be a track-and-hold as opposed to a sample-and-hold. The AFE timing may then be changed such that one sample of the discriminator outputs is made in the middle of the integration window and registered inside the CPLDs, and then a second is made one crossing (132 nsec) later after the S/H has dropped and the SIFT outputs are held.

The first, or 'early', sample, is multiplexed and stored within the VSVX_MUX's Event Delay FIFO during the crossing that contains the integration window. The second, or 'late' sample – actually taken at the end of the integration window but held by the S/H – is held at the output of the SIFT until the next crossing where it is then transferred into the VSVX_MUX and stored into the FIFO. In short, the current implementation of the logic samples the SIFT once and stores it into the Event Delay FIFO in one of the three 132 nsec period of the 396 nsec cycle. The new implementation would sample the SIFT twice during the integration window (middle and end) and use 264 nsec of the 396 nsec cycle to store the data into the Event Delay FIFO. A very quick sketch of this idea is shown in Figure 1.

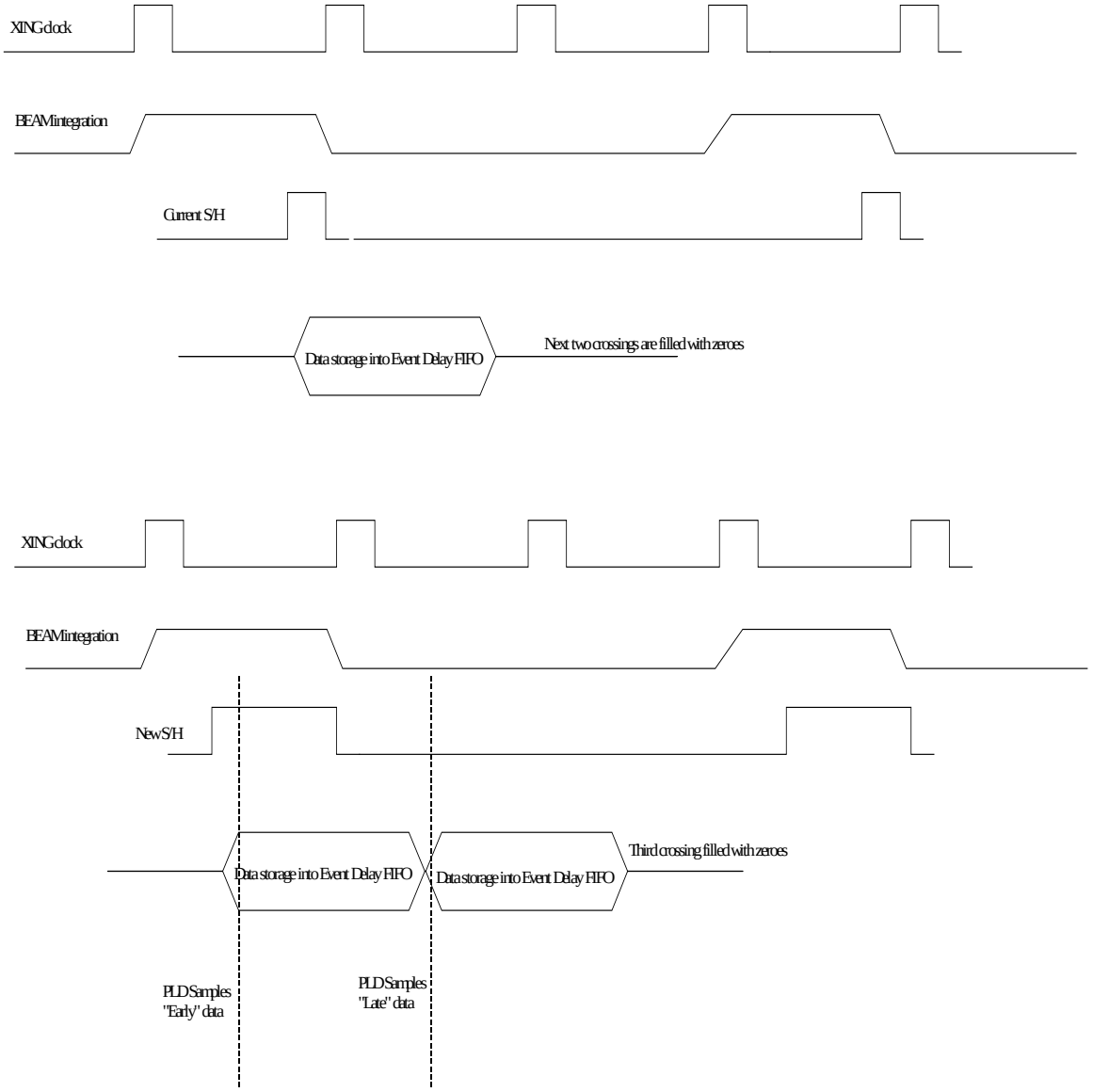

Figure 1

None of the main system timing need change. The specific list of changes required is:

- The timing of the event trigger from the Clockgen PLD to the MUX PLDs will have to be moved earlier.
- The S/H pulse timing in the Clockgen PLD would change.
- The logic in the VSVX_MUX would change to implement the holding register.
- The logic in the VSVX would change to support a longer readout.

Effects upon the trigger and readout deadtime

The LVDS_MUX PLDs could implement the same sort of changes as discussed above to send duplicate data to the DFE boards, but the utility of sending 'early hit' and 'late hit' data to the DFEs is questionable. If naught else, asking the DFE to take this information into account will introduce a serious time penalty (up to 132 nsec). The more likely implementation is to do this only in the VSVX subsystem. Reading out twice the discriminator information in the VSVX readout would, of course, increase the readout deadtime by adding another 130 bytes (Chip ID, status, and 64 address/data pairs) to the readout. At a readout rate of 40 MHz the deadtime would be increased by 3.25 usec. This may be alleviated by packing the data differently in the VSVX. Since there is no zero suppression in the VSVX the 'address' information is redundant once the pattern is known. Thus, the logic could be designed such that the extra bits are sent in lieu of the address information in a fixed format; this would result in no deadtime penalty.

Accuracy Considerations

While the algorithm may appear interesting at first glance, initial excitement must be tempered due to the way the SIFT discriminator works. There is significant time walk in the discriminator based upon how much the incoming charge exceeds the discriminator threshold. Thus, correction factors based upon the SVX measurement of the total charge will be required to compensate for this. A second accuracy concern is that holding the S/H switch closed for longer periods may adversely affect the SVX measurement itself. A 'back of the envelope' look at the circuit suggests that the errors introduced should be small and manageable, but tests will be required. Third, the SIFT output has time constants and known glitches that may corrupt the 'early' information. Engineering studies will be required to insure that the double-sampling is valid. One possibility to consider in this regard is using the S/H during a non-populated crossing to always reset all the SIFT outputs to zero, minimizing the time difference between $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions.

Costs to Implement this Algorithm

Besides the design effort, large amounts of testing and characterization to insure that all SIFT channels behave in similar ways is required. Further, detailed studies of the effect of changing the S/H signal on the SVX accuracy are required. What may not be obvious is that the PLD changes necessary to implement this algorithm will also increase the power load each AFE presents to the bulk power supply system. An increase of 5% in the +3.3V power draw may be expected, with the attendant increase in heat load on the platform.

Algorithm Expansibility

No more than one bit of time-of-flight information can be obtained with the current hardware. Insufficient resources exist in the PLDs to sample the discriminator information more than once in addition to the 'free' latch provided by the SIFT. It may be possible to offset the time of the 'early' sample in the VSVX_MUX relative to the 'early' sample taken in the LVDS_MUX, but there exists no possibility to transfer this information between the two PLDs within the required time intervals.

Proposal for Continued Work

Pursuing this idea seems a valid effort if Monte Carlo simulations of the detector indicate that splitting the hit data into 'north' and 'south' halves for all Axial fibers is useful. If nothing else, even a partial determination of Z information may provide sufficient seeding information to allow for extraction of better Z data from the stereo fibers. Engineering work to detail the operability of the algorithm is not recommended until Monte Carlo simulations indicate that the excess information is valuable for tracking purposes. Should such simulations pan out, then tests at the Phase V test stand using the AFE Test Module and a programmable delay box will be more than sufficient to yield the actual ability to measure time-of-flight and to characterize the consistency of SIFT discriminator time response over large numbers of channels.